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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,129	04/15/2004	Huilong Zhu	FIS920030413	3128

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EXAMINER	
HOANG, QUOC DINH	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,129	ZHU ET AL.	
	Examiner	Art Unit	
	Quoc D. Hoang	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-16* is/are allowed.

6)☒ Claim(s) *1-7 and 9-11* is/are rejected.

7)☒ Claim(s) *8,12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Examiner withdraws the previous election/restriction on 08/24/2006. Claims 1-18 are pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-7, 9, 10, 11, 17 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Skotnicki et al., (US Pat No. 6,727,186 hereinafter "Skotnicki").

Regarding claim 1, Skotnicki teaches a method of producing a fin structure, the method comprising:

providing a semiconductor substrate 12, an SiGe layer 14 on said semiconductor substrate 12, and a silicon layer 15 on said SiGe layer 14 (col. 4, lines 30-47 and Fig. 2);

defining a fin portion of said silicon layer 15, said fin portion having thereunder a second portion of said SiGe layer 14 (col. 4, lines 30-47 and Fig. 2); *Note that the portions 14/15 are defined between insulative box 13 (see Fig. 2).*

forming a support structure 24 attached to said fin portion 15 and said semiconductor substrate 12 (col. 5, lines 19-21 and Fig. 3); and

removing said second portion 14 to form a first void 27 between said fin portion 15 and said semiconductor substrate 12 (col. 5, lines 22-34 and Fig. 4a); and

removing at least a portion of the support structure 24 (col. 5, lines 22-34 and Fig. 4a).

Regarding claim 2, Skotnicki teaches wherein said support structure 24 comprises portions of said SiGe layer 14 not part of said second portion, and portions of said silicon layer 15 not part of said fin portion (col. 5, lines 19-34 and Fig. 4a).

Regarding claim 3, Skotnicki teaches wherein said support structure comprises a spacer material (col. 5, lines 19-21 and Fig. 3).

Regarding claim 4, Skotnicki teaches wherein said support structure is selected from the group consisting of oxide (col. 5, lines 19-21).

Regarding claim 5, Skotnicki teaches wherein said support structure comprises a gate 19 of a field effect transistor (col. 4, lines 48-65).

Regarding claim 6, Skotnicki teaches wherein said defining and forming steps are simultaneous (col. 4, lines 32-47 and Fig. 2).

Regarding claim 7, Skotnicki teaches wherein said support structure 24 comprises portions of said SiGe layer 14 not part of said second portion, and portions of said silicon layer 15 not part of said fin portion (col. 5, lines 19-34 and Fig. 4a).

Regarding claim 9, Skotnicki teaches wherein said step of removing said second portion 14 comprises selectively wet etching said second portion 14 (col. 5, lines 28-33 and Fig. 4a).

Regarding claim 10, Skotnicki teaches a method of producing a fin structure, the method comprising:

providing a semiconductor substrate 12, an SiGe layer 14 on said semiconductor substrate 12, and a silicon layer 15 on said SiGe layer 14 (col. 4, lines 30-47 and Fig. 2);

defining a fin portion of said silicon layer 15, said fin portion having thereunder a second portion of said SiGe layer 14 (col. 4, lines 30-47 and Fig. 2); *Note that the portions 14/15 are defined between insulative box 13 (see Fig. 2).*

forming a support structure 24 attached to said fin portion 15 and said semiconductor substrate 12 (col. 5, lines 19-21 and Fig. 3); and

removing said second portion 14 to form a first void 27 between said fin portion 15 and said semiconductor substrate 12 (col. 5, lines 22-34 and Fig. 4a);

deposting an insulating material 27 in said first void (col. 5, lines 34-37 and Fig. 4b); and

removing the support structure 24 (col. 5, lines 22-34 and Fig. 4a).

Regarding claim 11, Skotnicki teaches the insulating layer is oxide (col. 5, lines 34-37 and Fig. 4b)

Regarding claim 17, Skotnicki teaches oxidizing said lower surface of said fin portion 15 after removing said second portion 14 (col. 5, lines 34-37 and Fig. 4b).

Regarding claim 18, Skotnicki teaches wherein the fin structure forms a part of a field effect transistor (col. 4, lines 48-65).

Allowable Subject Matter

4. Claims 14, 15 and 16 are allowed.

5. Claims 8 and 12-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

None of the references of record teaches or suggest the claim method of producing a fin structure having the steps of depositing a first blocking layer on said silicon layer; depositing a poly-silicon layer on said first blocking layer; patterning said poly-silicon layer and said blocking layer to reveal a first portion of said silicon layer and a first portion of said SiGe layer and producing a sidewall of said polysilicon layer and a sidewall of said first blocking layer; forming a first spacer on said sidewall of said poly-silicon layer and said sidewall of said first blocking layer to cover said first portion and said second portion; removing said first portion of said silicon layer to form a first sidewall of said silicon layer while said fin portion remains; removing said SiGe layer to form a first sidewall of said SiGe layer while said second portion remains; and forming a second spacer on said sidewalls of said polisilicon layer, said first blocking layer said silicon layer, and said SiGe layer.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quoc Hoang whose telephone number is (571) 272-1780. The examiner can normally be reached on Monday-Friday from 8.00 AM to 5.00 PM.

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MinSun Harvey can be reached on (571) 272-1835. The fax phone numbers of the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quoc Hoang
Patent examiner/AU 2818

09/23/2006